Test Methodology for the McKinley Processor

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Purpose of Work

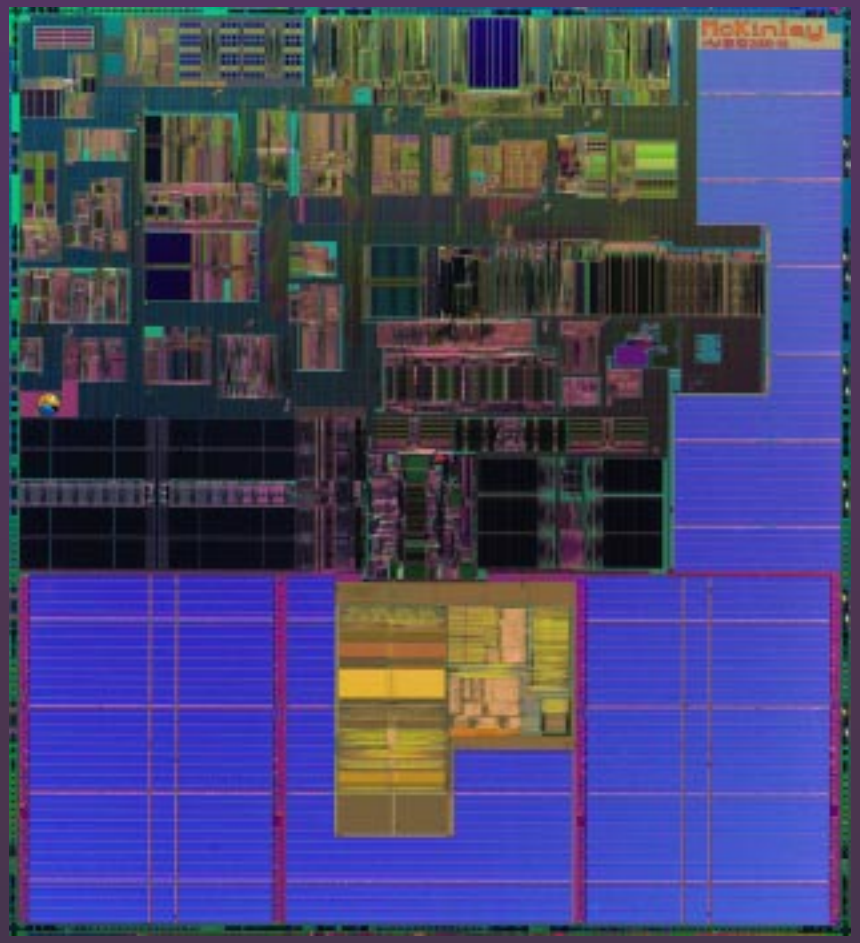
- Enable testability for McKinley
- Deliver a high quality test solution
- Investigate new test features
- Learn for the future

Presentation Overview

- McKinley overview
- Test methodology
- Test controller
- Scan methodology
- Array testing
- Results/conclusions

McKinley Overview

- Intel/HP designed
- New microarchitecture
- 221 million FETs
- 1 GHz operation
- 8 stage pipeline
- 6 wide super scalar
- 11 issue ports
- 3 levels of cache
- 400 MT/s bus



Test Methodology Goals

- Reduce design impact of adding test
- Enable fast, efficient analysis of functional and electrical bugs
- Reduce engineering time needed for pattern generation
- Increase quality and coverage of manufacturing test
- Keep test methodology simple and consistent

Test Methodology

- Increased on-chip support for test
- Nearly full scan design
- Direct Access Test (DAT)
  - For 13 arrays over 4 KB
- Burn-in support for toggle coverage

Integrated Test Controller

- Supports IEEE 1149.1 Standard
- 84 instructions
- Distributed “minitaps”
  - TCK routed by balanced H-tree
  - Local buffering of test signals
  - Selection between ITC or bus for data
  - Serial or parallel access to scan chains

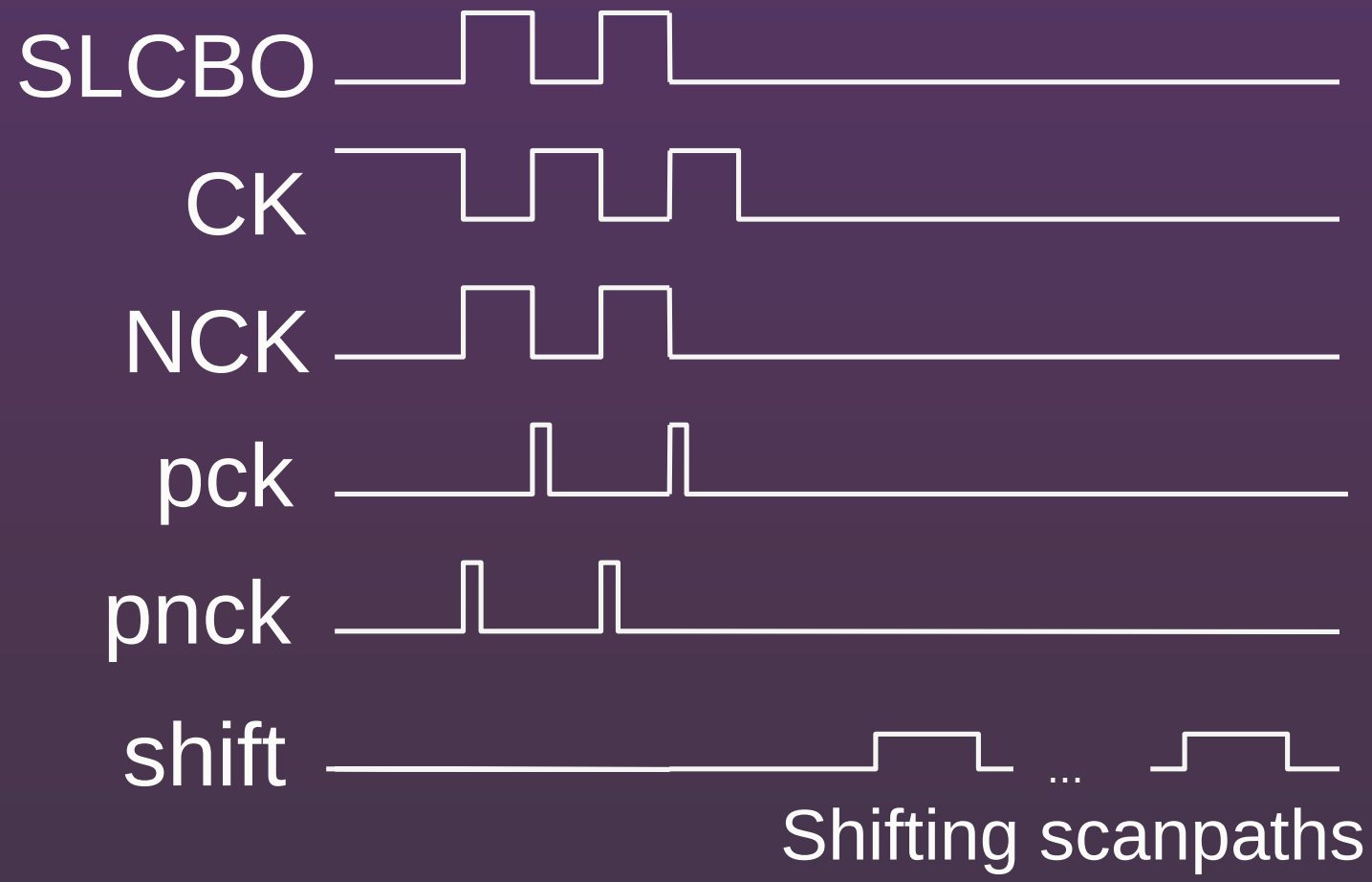
Scan Methodology

- Overcome circuit design complexity
- 51 total scan paths – 36 used for ATPG
- 136,000 state elements scanned
  - Roughly 85% of non-memory state
  - Most unscanned structures were queues
- 24,000 additional scanlatches
  - Used for non-invasive debug

Clocking

- Design uses pulse latches
- Single clock throughout design
  - Regions controlled by “gaters”
  - Gated clocks enabled via qualifying signal
  - Generates pulsed pck/pnck or dynamic CK/NCK clocks

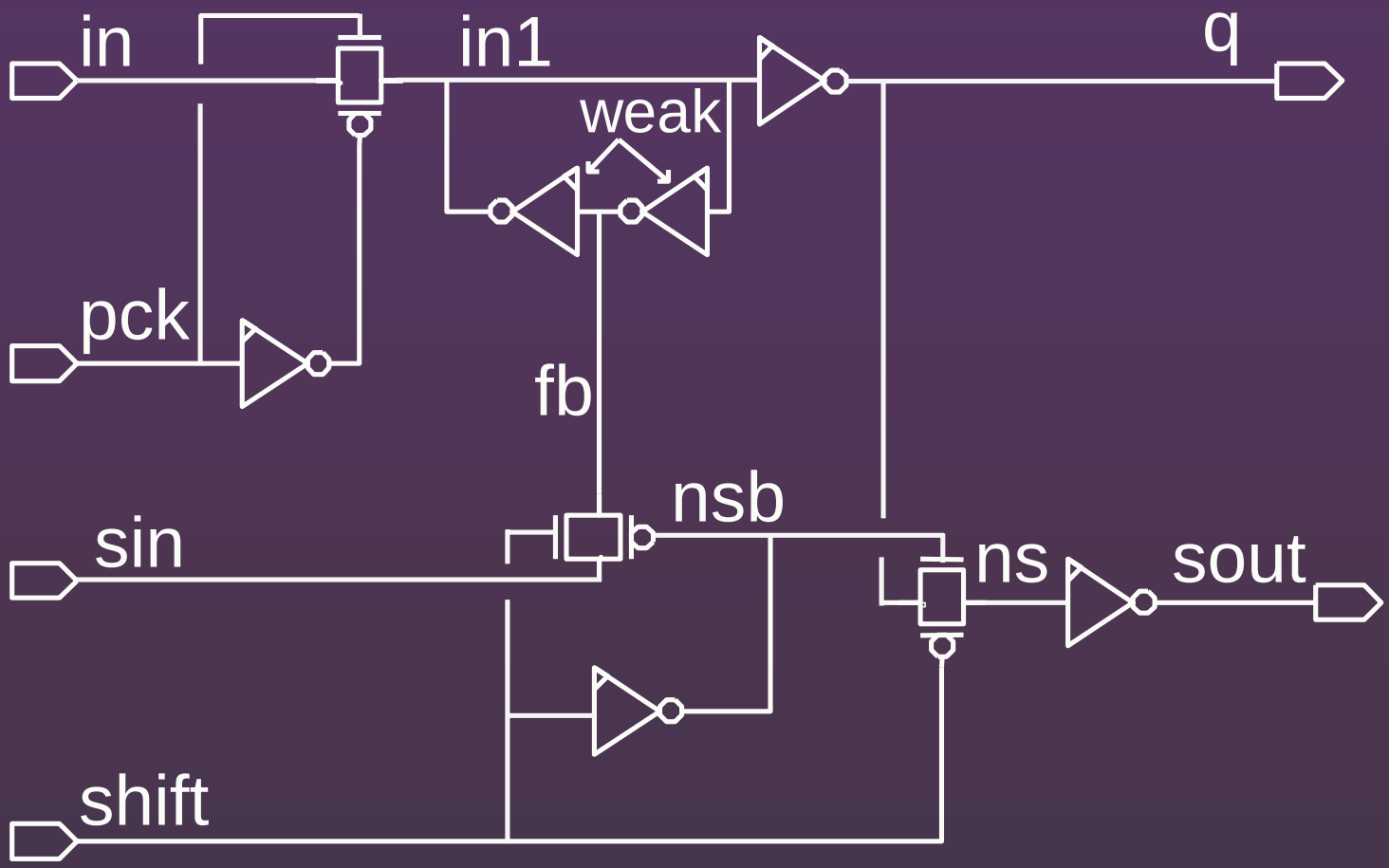
Clocking Diagram



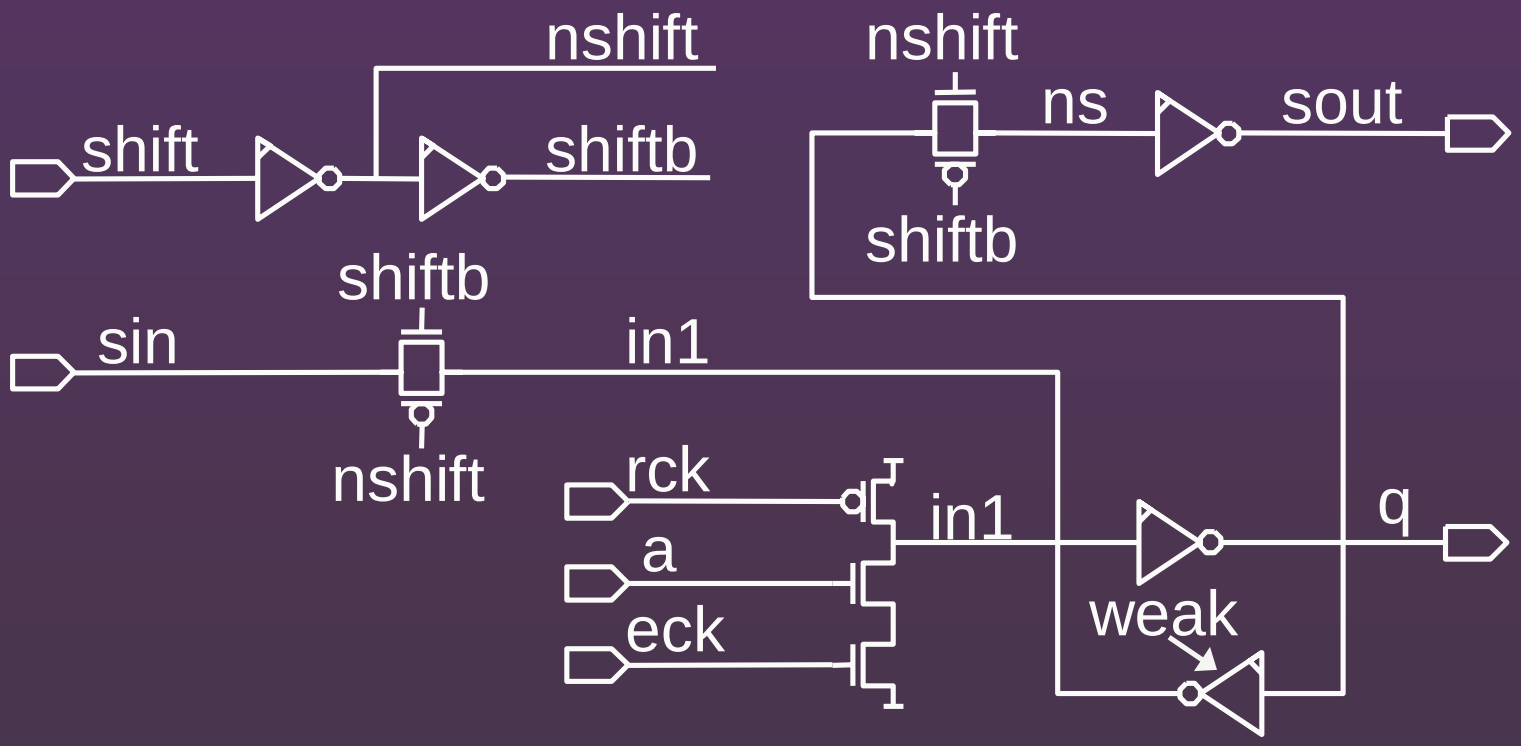
Scan Latch Design

- Static latches are pulse latches
- Last dynamic gate has a dynamic latch converter
  - Separate precharge and evaluate clocks
  - Keeper to hold value during next phase
- Clock stopped low for scan shifting
- Clock is stepped single/multiple times
  - Provides stuck at and delay fault testing

Static Latch Schematic



Dynamic Latch Schematic



Scan Chain Shifting

- Minitaps generate shift based on TCK
- Test signal gates some “wiggle” signals
- Only NCK dynamic latches are not scanned

Scanlatch Design

- Advantages
  - Small number of wires: shift and data
  - 20% area impact per latch
  - 0.5% total area impact for die
- Disadvantages
  - Outputs “wiggle” during shifting
  - Leakage on ns node
  - Race between scan latches
  - Additional power

Scan Verification

- Template-based SPICE evaluation tool
- Netlist stitching tool for early ATPG
- Ability to back annotate artwork
- Switch level simulation for continuity
- SPICE simulations of shift clock

ATPG Modeling

- Started as schematics completed to identify issues
- Dynamic circuits
  - Converted to combinational equivalents
  - Hand remodeling needed for stuck at coverage level

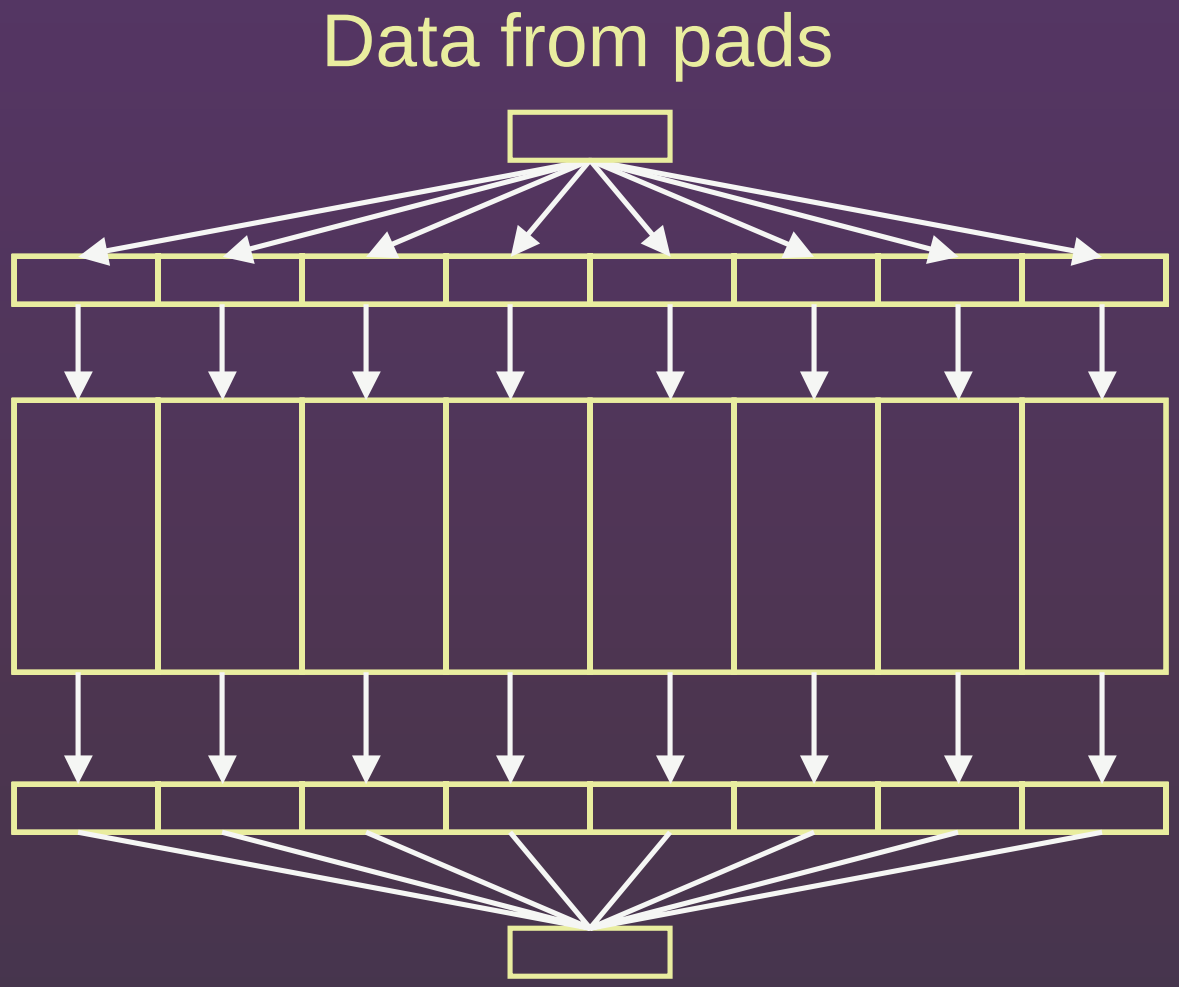
Array Testing

- Direct Access Testing (DAT)
- Three levels of cache hierarchy
  - 3 MB L3
  - 256 KB L2
  - Single cycle L1D and L1I (16 KB each)
- Approximately 75% of transistors in RAM or CAM cells
- Used existing data and control paths

Array Testing

- Register for selecting test setup
- 32 input pads replicated to fill cache line
- Read return data returned to 32 pads
- Set, way and commands from pads
- Cache line data compared to “golden” 32-bit chunk
- Runs at full speed

Replicated/Sticky Bit Compare



Replicated data

Data to/from array

Captured read data

DAT modes

- DAT write/reads/nops
- Diagnose for individual bit control
- Init mode for clearing/initializing arrays
  - Used for toggle coverage in burn-in
- BIST for two largest data arrays
- Modes accessible via code or JTAG

Silicon Results

- All test circuitry fully functional at first silicon
- Scan paths work from 1 to 150 MHz+
- ATPG patterns are passing
- DAT functional on all arrays
  - Excellent manufacturing test coverage
  - Used to characterize array issues
- Minor issues with boundary scan chain

Conclusion

- McKinley test methodology challenging
  - New circuit design techniques
  - Complex design
- Met test methodology goals
- Minimal impact on design team
- Scan/DAT enabled quick debug
- We acknowledge the exceptional contributions of our colleagues!